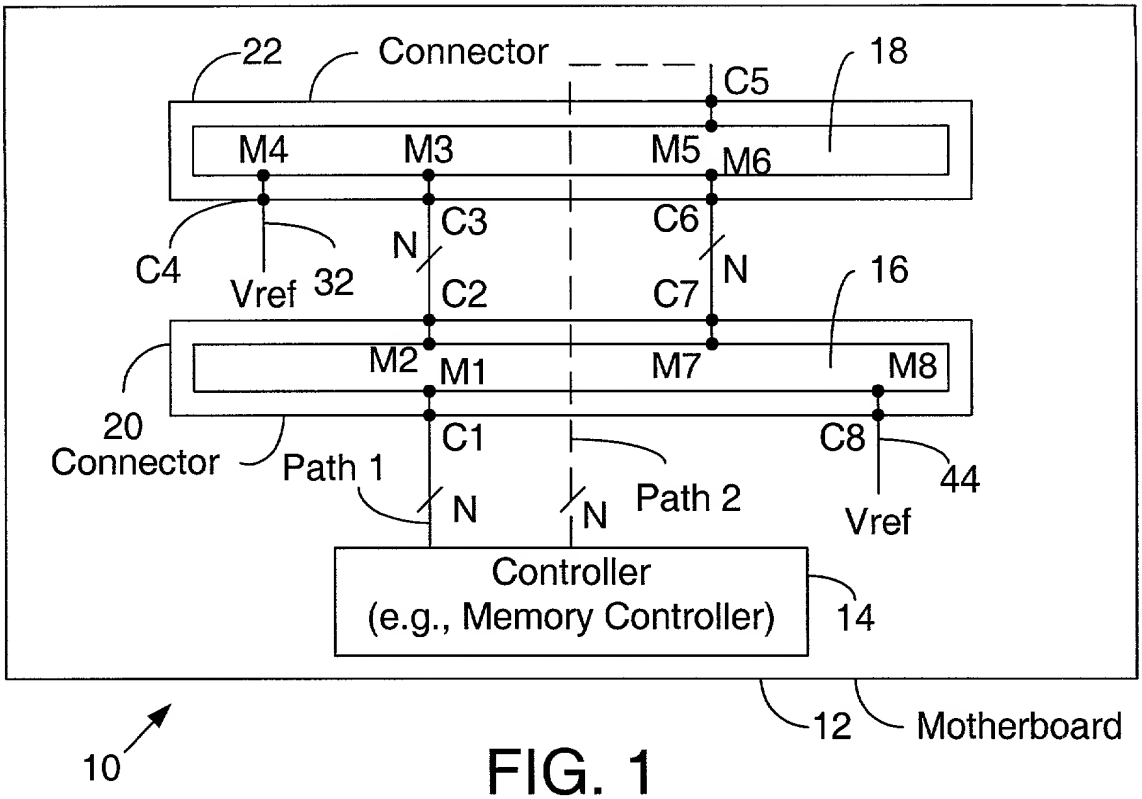
22
Connector
C5
18
M4
M3
M5
M6
C4
Vref
32
N
C3
C2
C6
N
C7
16
M2
M1
M7
M8
20
Connector
Path 1
C1
N
N
Path 2
C8
44
Vref
Controller
(e.g., Memory Controller)
14
12
Motherboard
10

FIG. 1

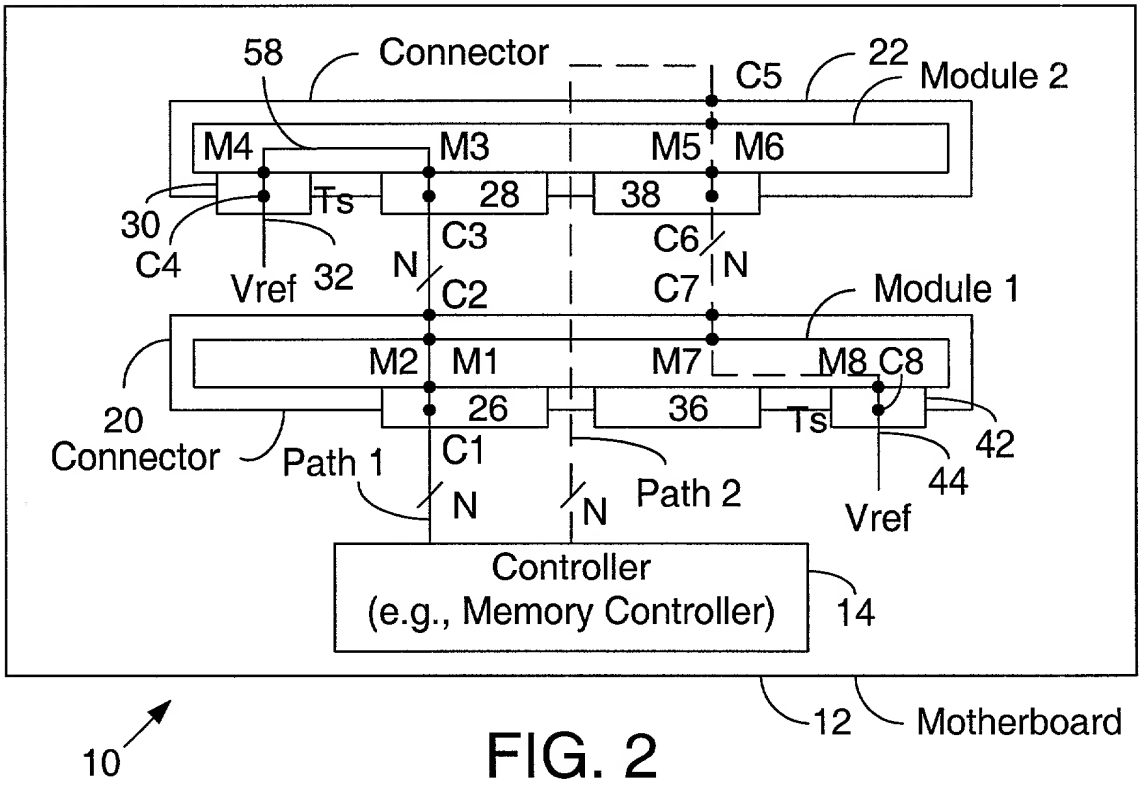
58
Connector
C5
22
Module 2
M4
M3
M5
M6
Ts
28
38
30
C4
Vref
32
N
C3
C2
C6
N
C7
Module 1
M2
M1
M7
M8
C8
20
Connector
Path 1
26
36
Ts
C1
N
N
Path 2
42
44
Vref
Controller
(e.g., Memory Controller)
14
12
Motherboard
10

FIG. 2

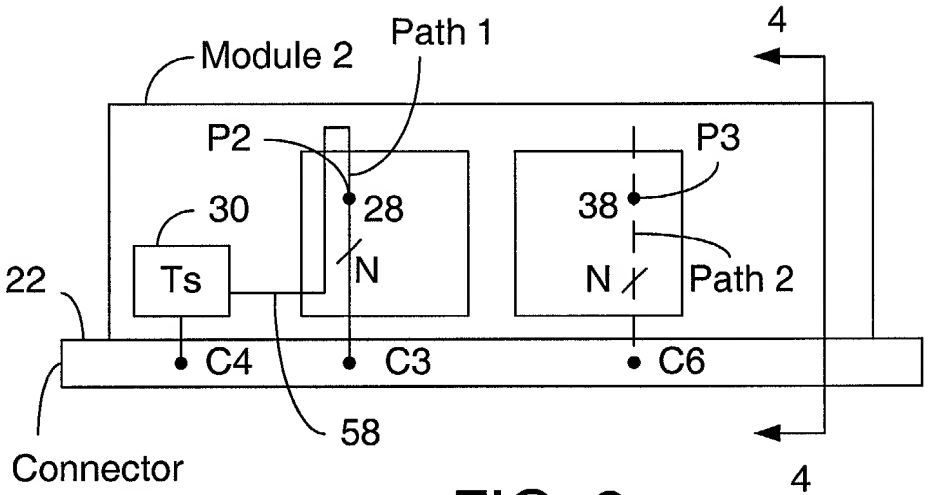

FIG. 3

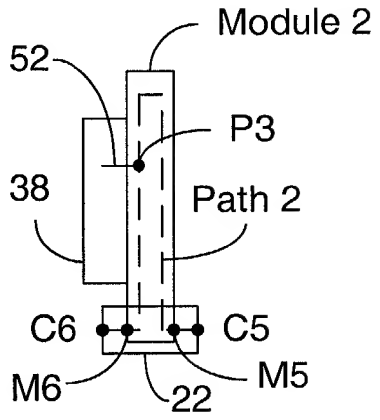

FIG. 4

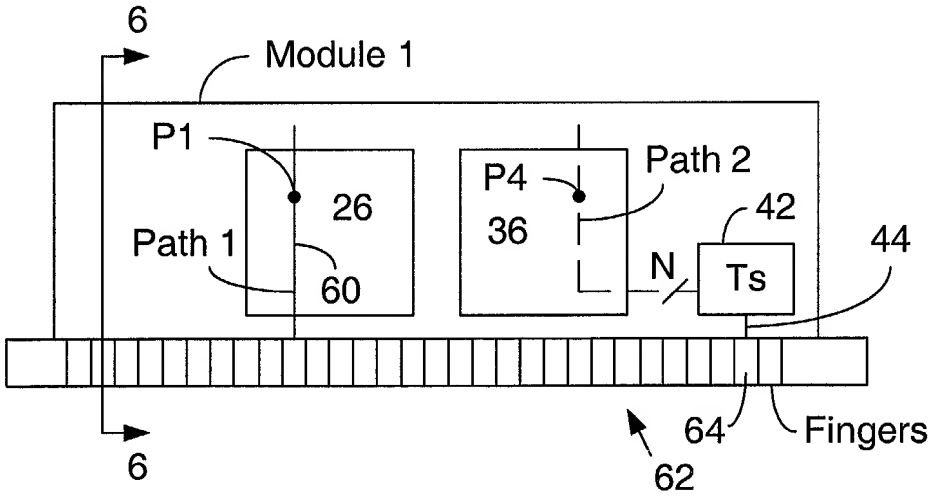

FIG. 5

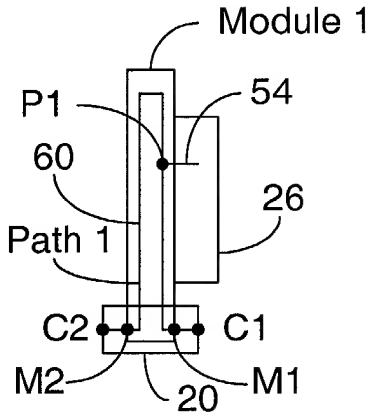

FIG. 6

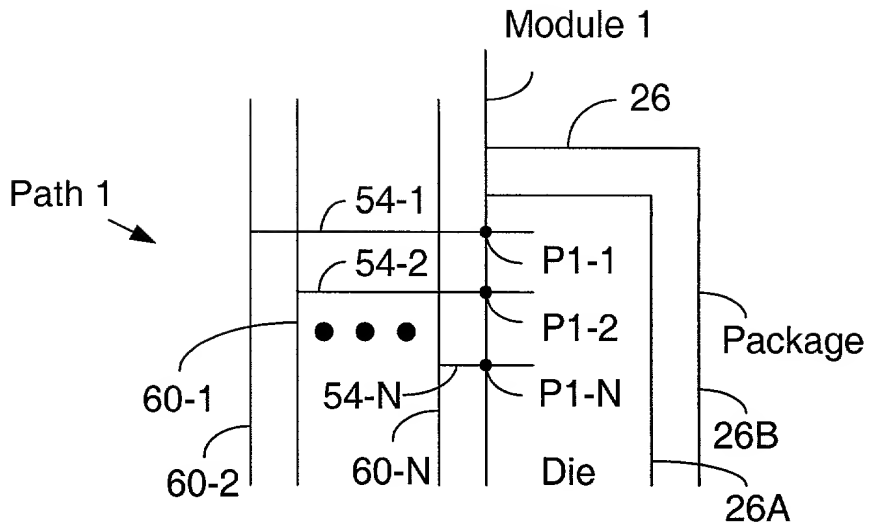

FIG. 7

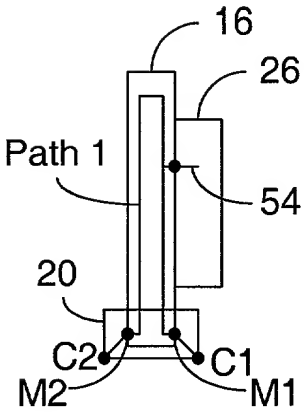

FIG. 8

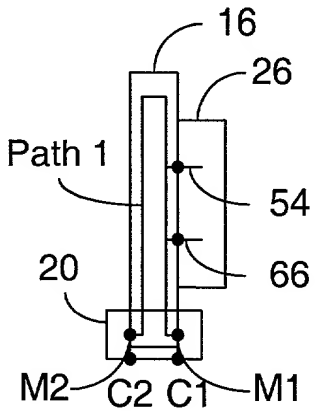

FIG. 9

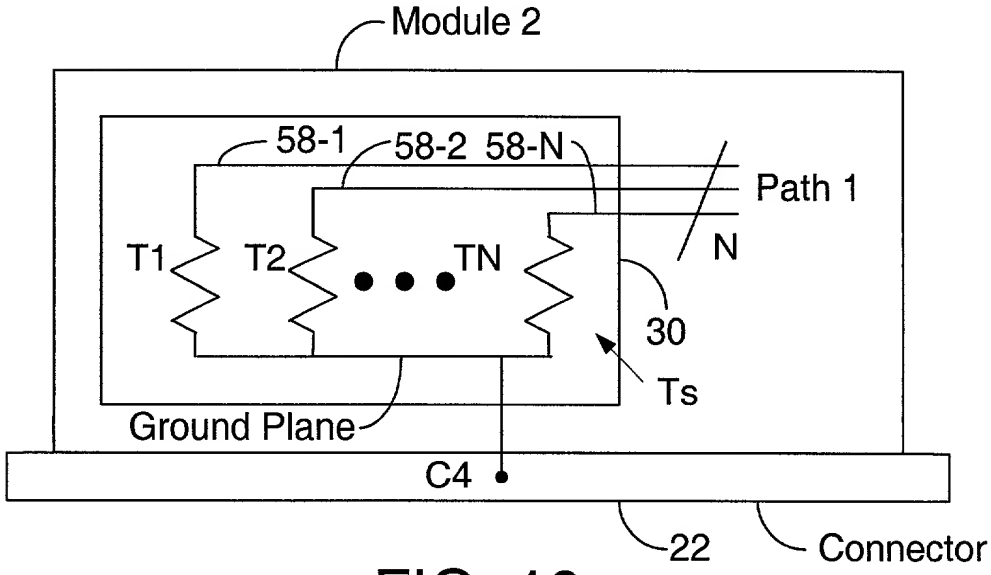

FIG. 10

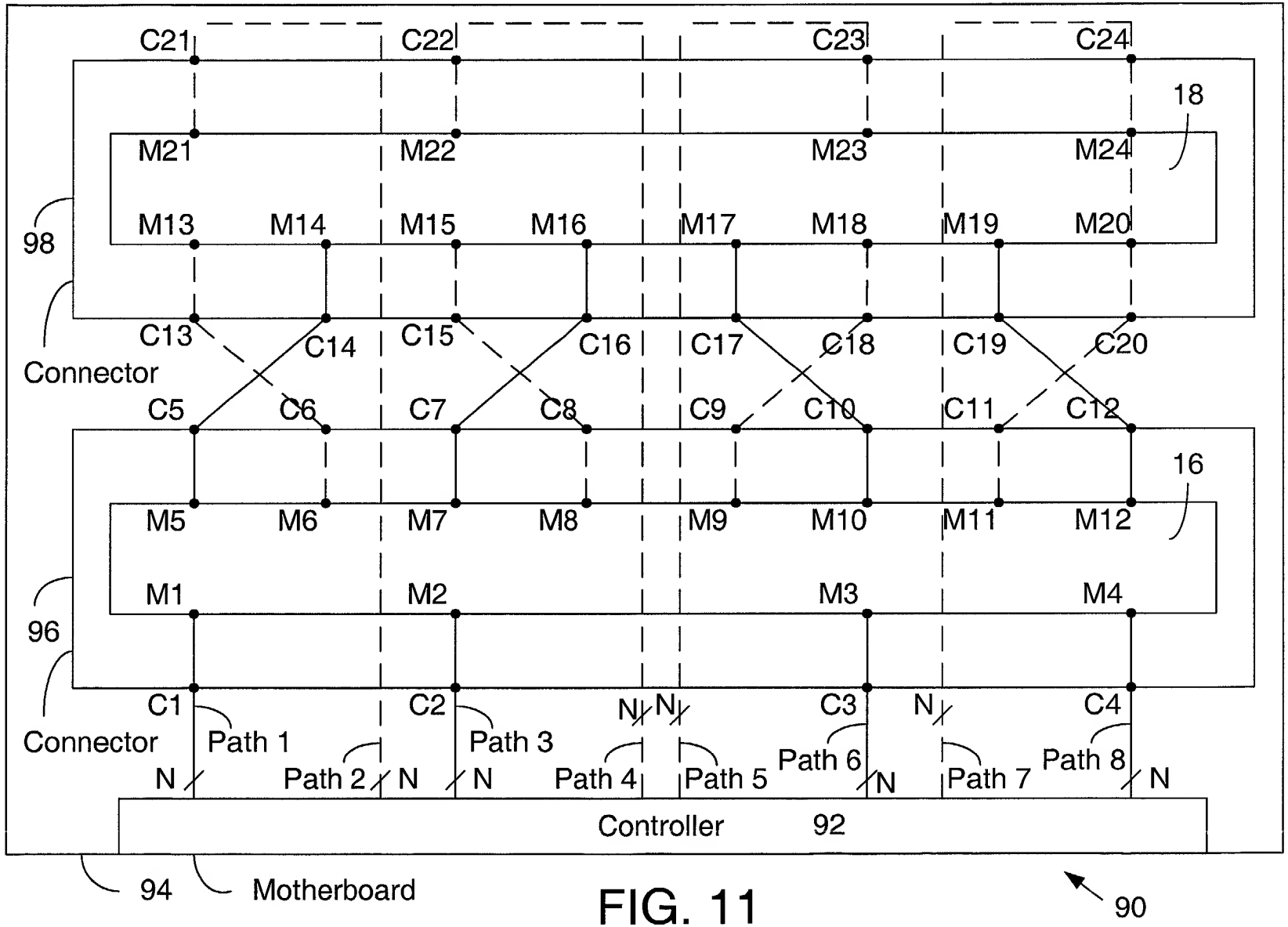

FIG. 11

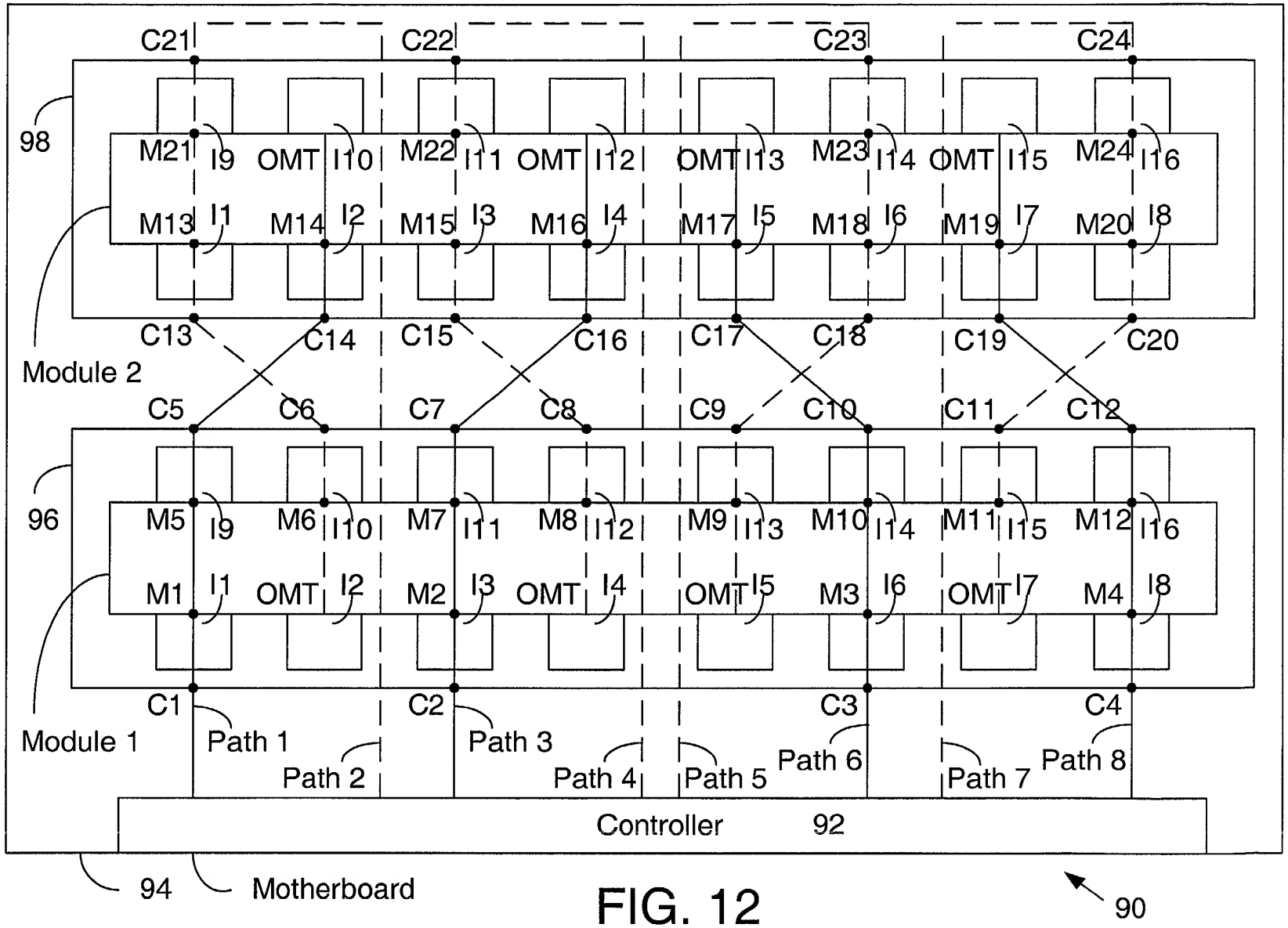

FIG. 12

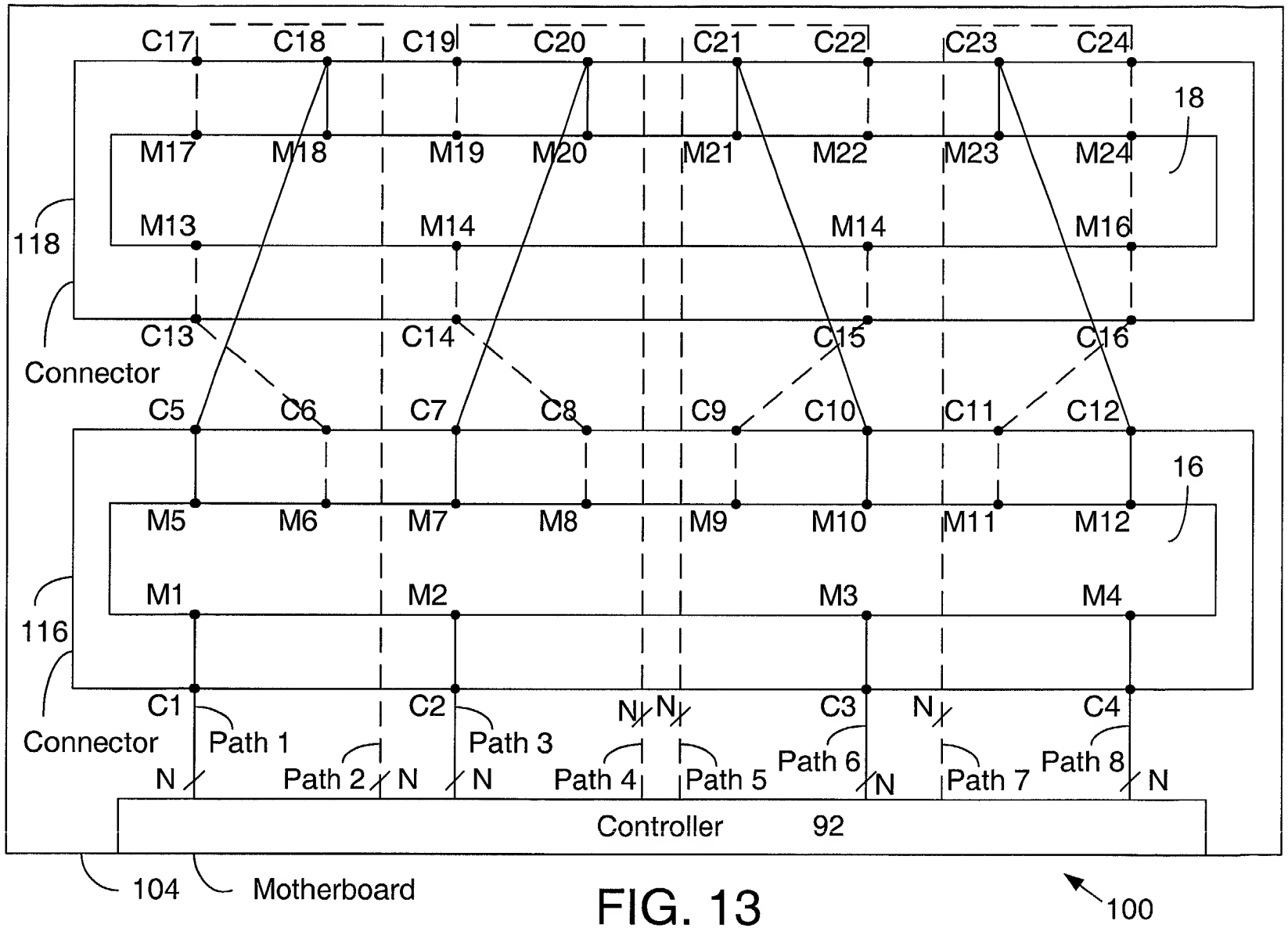

FIG. 13

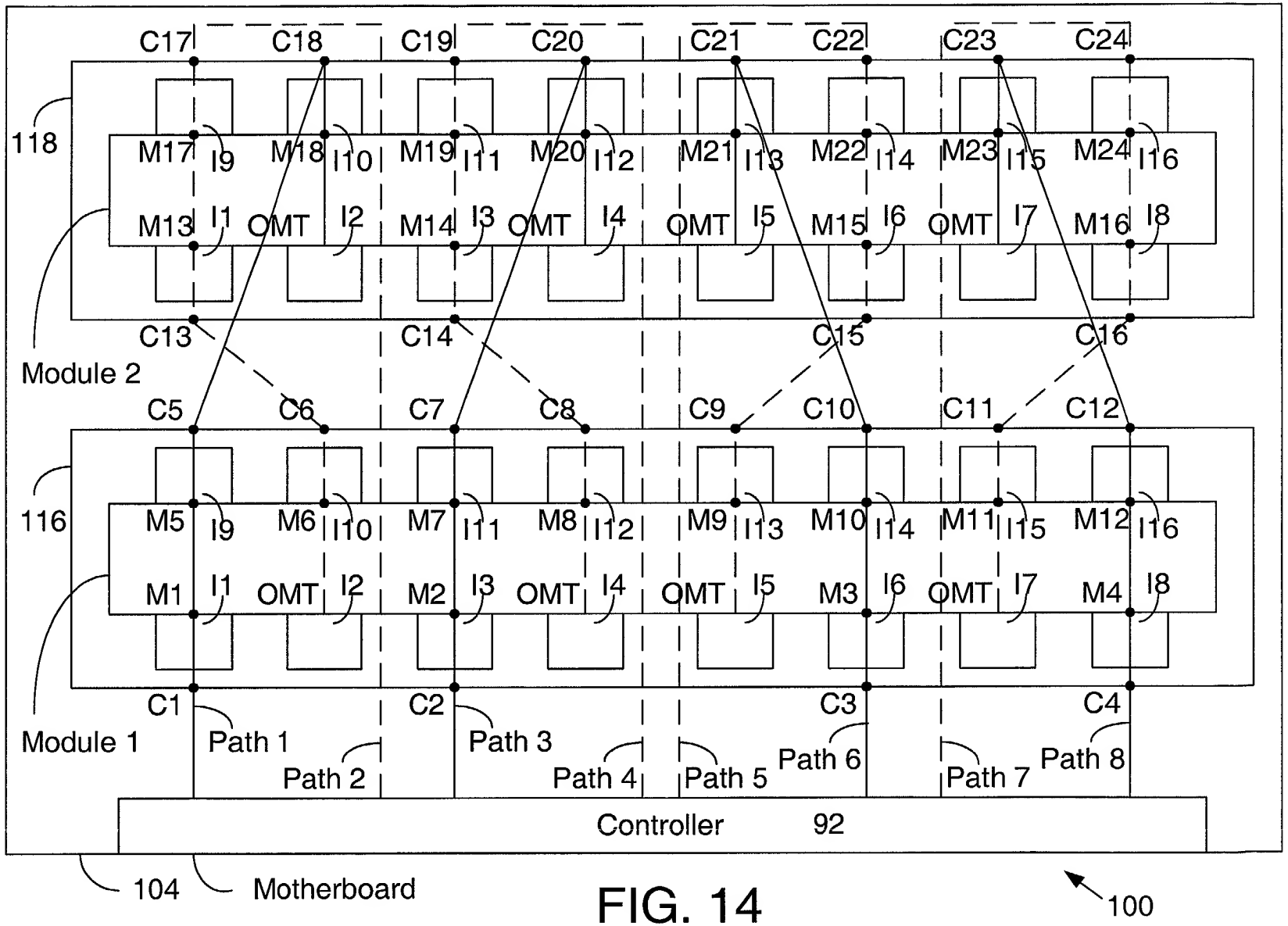

FIG. 14

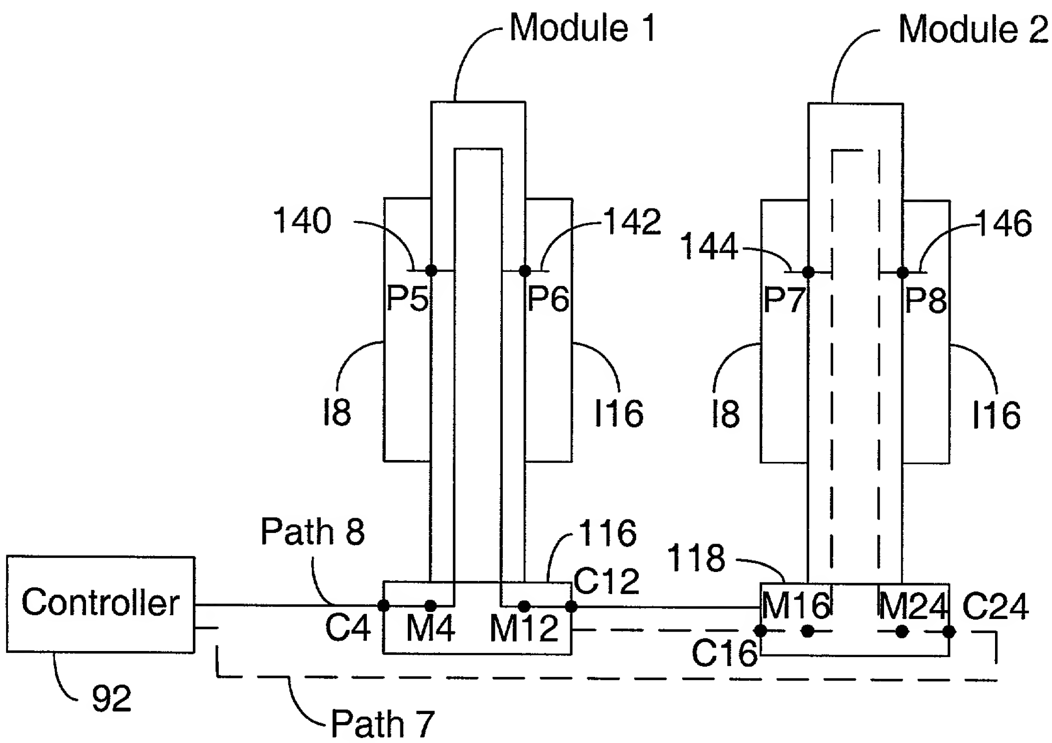
Module 1
Module 2
140
142
144
146
P5
P6
P7
P8
I8
I16
I8
I16
Path 8
116
118
C12
Controller
C4
M4
M12
M16
M24
C24
C16
92
Path 7

FIG. 15

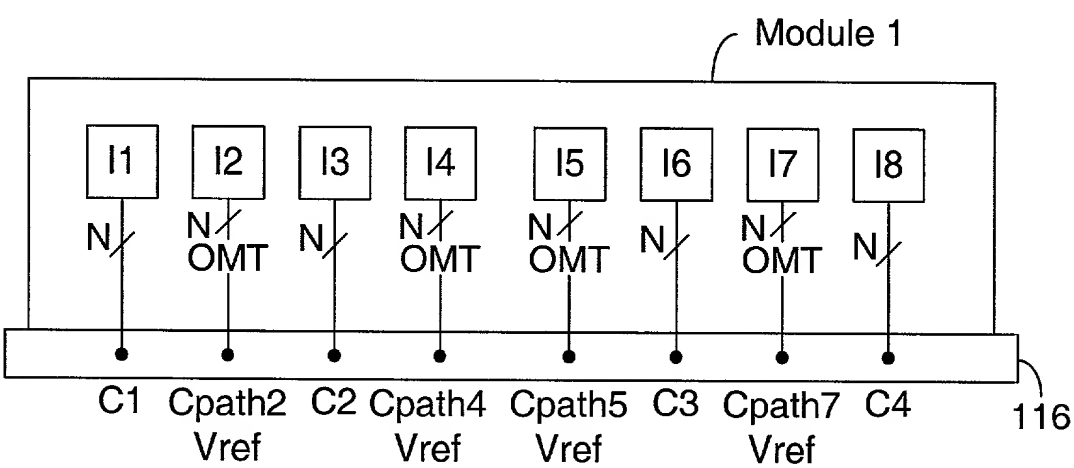
Module 1
I1
I2
I3
I4
I5
I6
I7
I8
N
N
OMT
N
N
OMT
N
OMT
N
N
OMT
N
C1
Cpath2
Vref
C2
Cpath4
Vref
Cpath5
Vref
C3
Cpath7
Vref
C4
116

FIG. 16

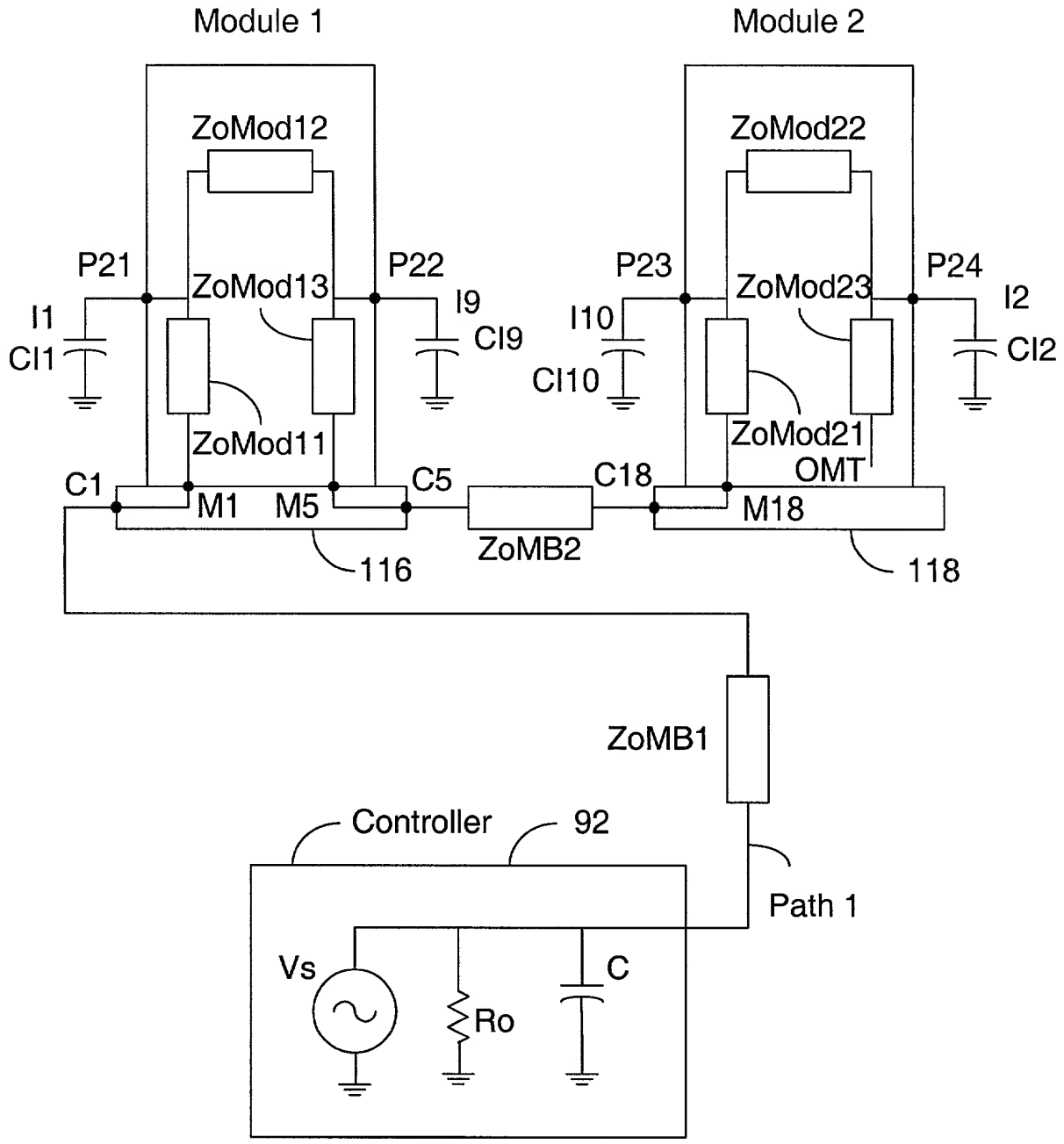
Module 1
Module 2
ZoMod12
ZoMod22
P21
P22
P23
P24
ZoMod13
ZoMod23
I1
CI1
I9
CI9
I10
CI10
I2
CI2
ZoMod11
ZoMod21
OMT
C1
C5
C18
M1
M5
M18
116
ZoMB2
118
ZoMB1
Controller
92
Path 1
Vs
Ro
C

FIG. 17

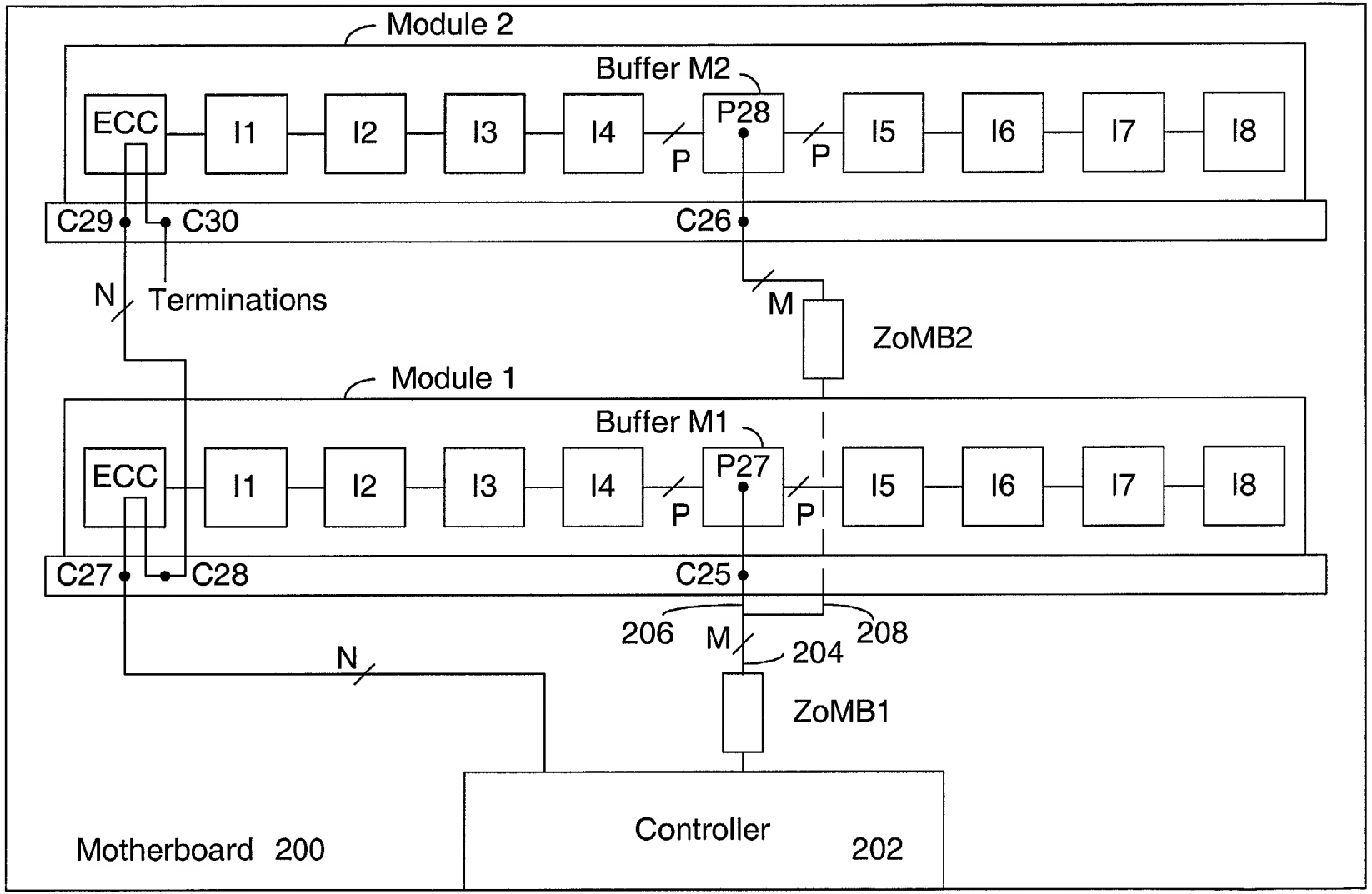
Module 2
Buffer M2
ECC
I1
I2
I3
I4
P28
I5
I6
I7
I8
P
P
C29
C30
C26
N
Terminations
M
ZoMB2
Module 1
Buffer M1
ECC
I1
I2
I3
I4
P27
I5
I6
I7
I8
P
P
C27
C28
C25
206
M
204
208
N
ZoMB1
Controller
202
Motherboard 200

FIG. 18

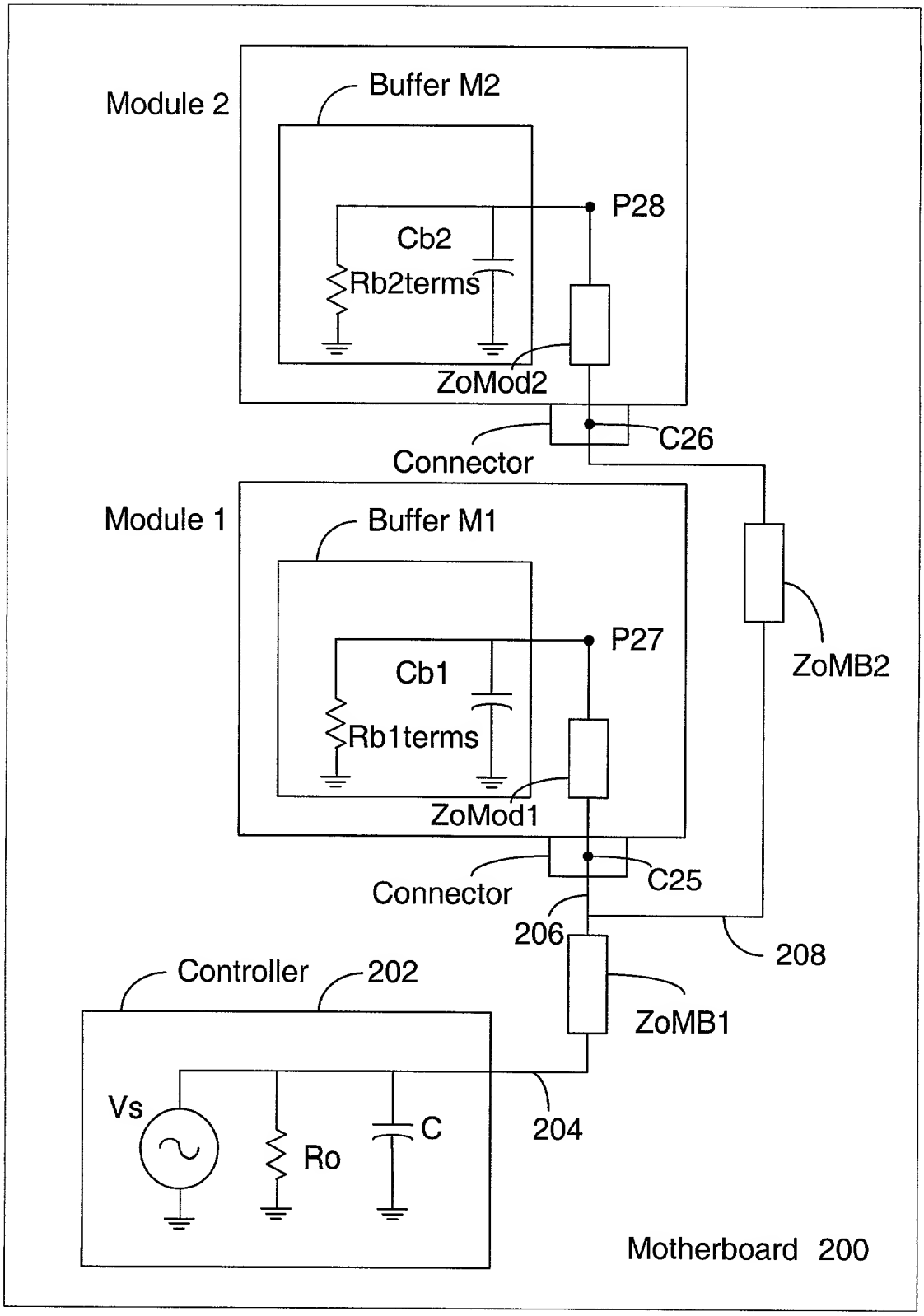
Module 2
Buffer M2
P28
Cb2
Rb2terms
ZoMod2
Connector
C26
Module 1
Buffer M1
P27
Cb1
Rb1terms
ZoMod1
ZoMB2
Connector
C25
206
208
Controller
202
ZoMB1
Vs
Ro
C
204
Motherboard 200

FIG. 19

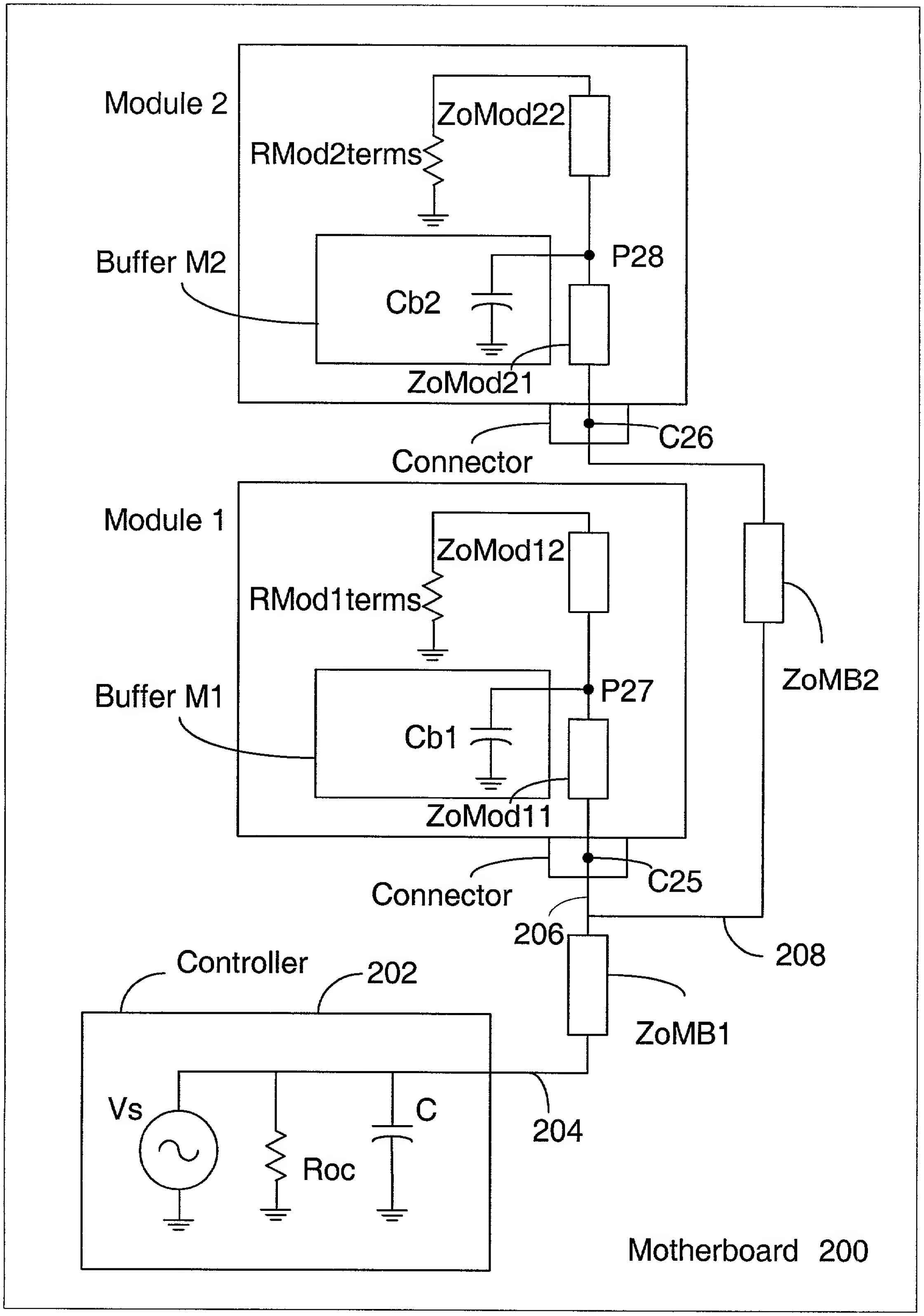

FIG. 20

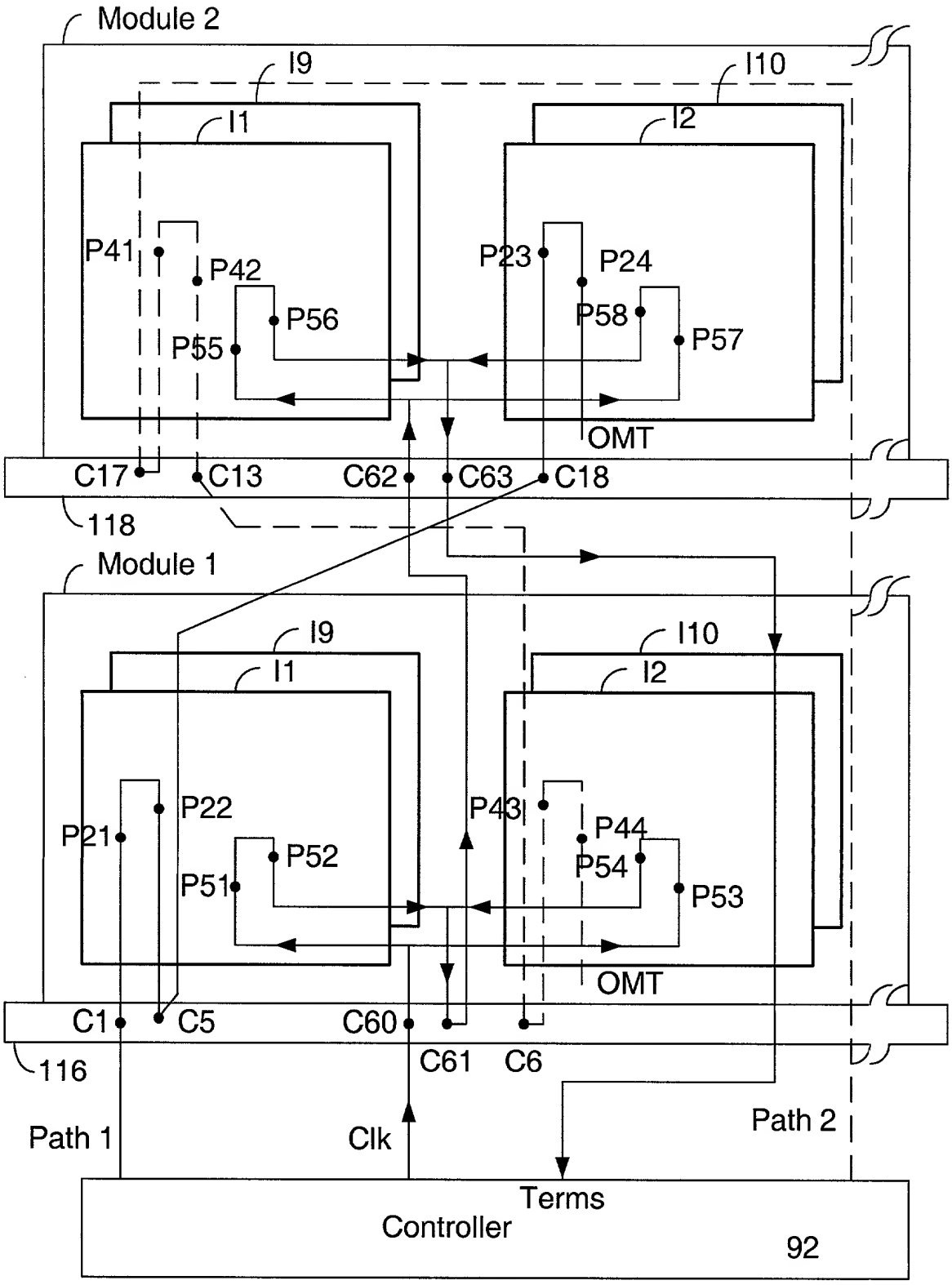
Module 2
I9
I10
I1
I2
P41
P42
P56
P55
P23
P24
P58
P57
OMT
C17
C13
C62
C63
C18
118
Module 1
I9
I10
I1
I2
P21
P22
P52
P51
P43
P44
P54
P53
OMT
C1
C5
C60
C61
C6
116
Path 1
Clk
Path 2
Terms
Controller
92

FIG. 21

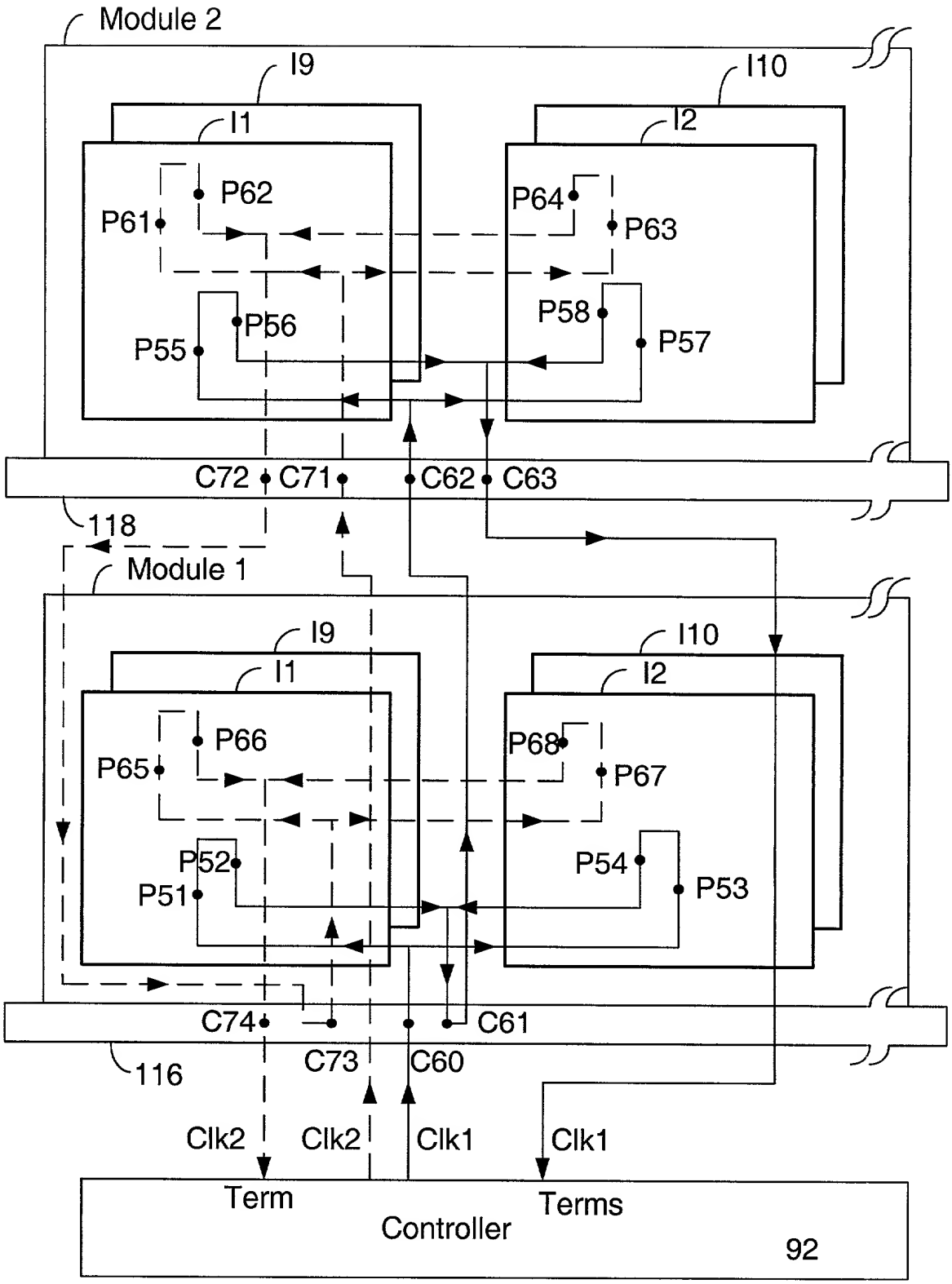
Module 2
I9
I10
I1
I2
P62
P61
P64
P63
P56
P55
P58
P57
C72
C71
C62
C63
118
Module 1
I9
I10
I1
I2
P66
P65
P68
P67
P52
P51
P54
P53
C74
C61
C73
C60
116
Clk2
Clk2
Clk1
Clk1
Term
Terms
Controller
92

FIG. 22

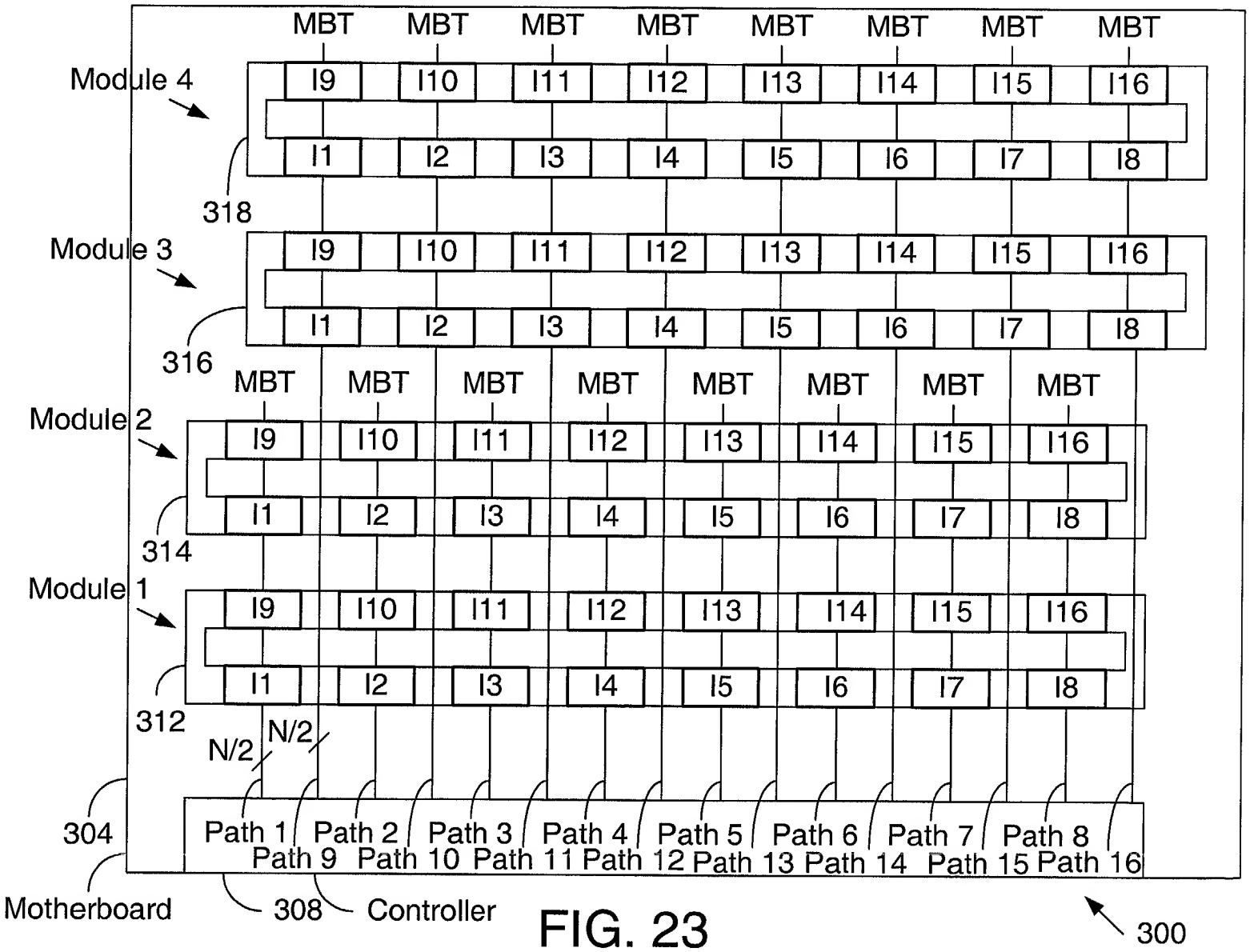

FIG. 23

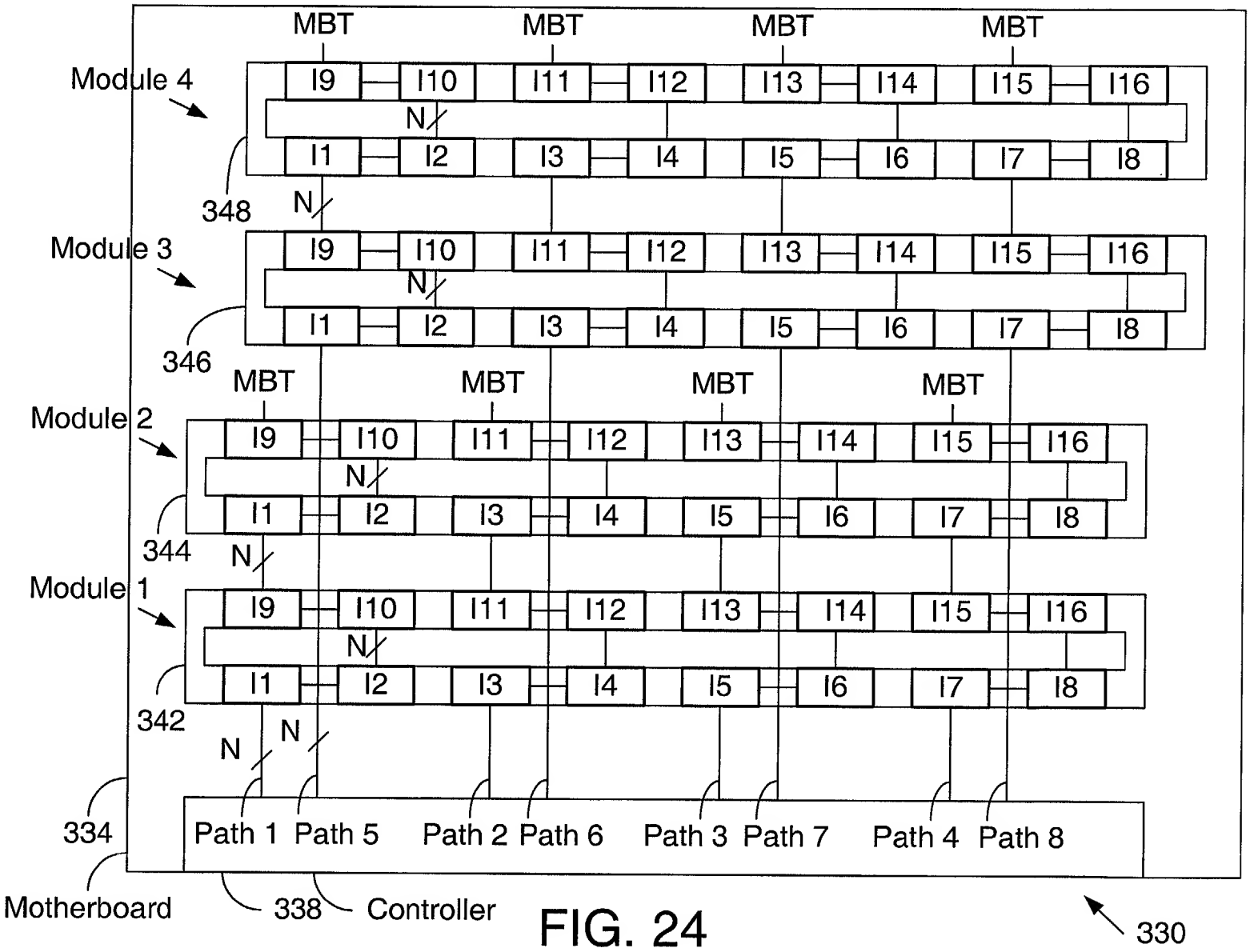

FIG. 24

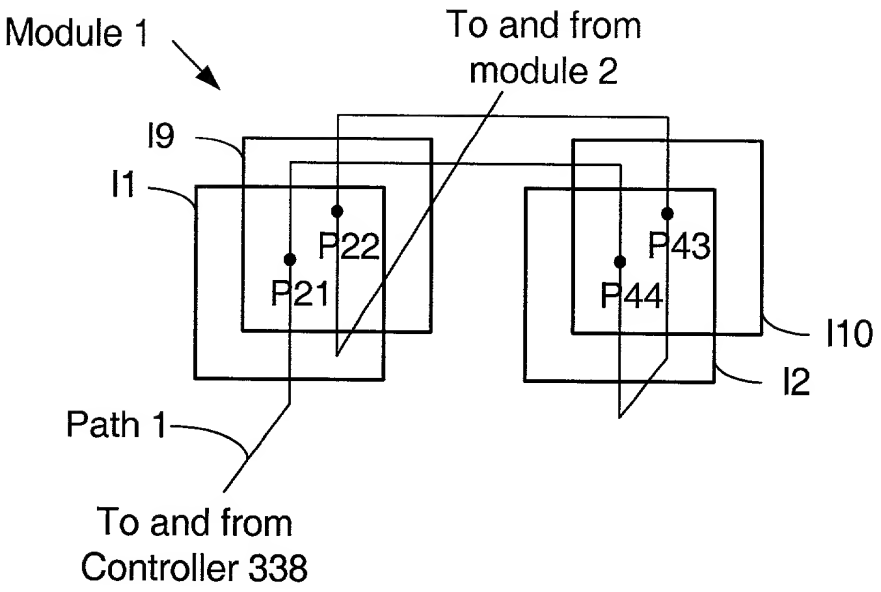
Module 1
To and from
module 2
I9
I1
P22
P21
P43
P44
I10
I2
Path 1
To and from
Controller 338

FIG. 25

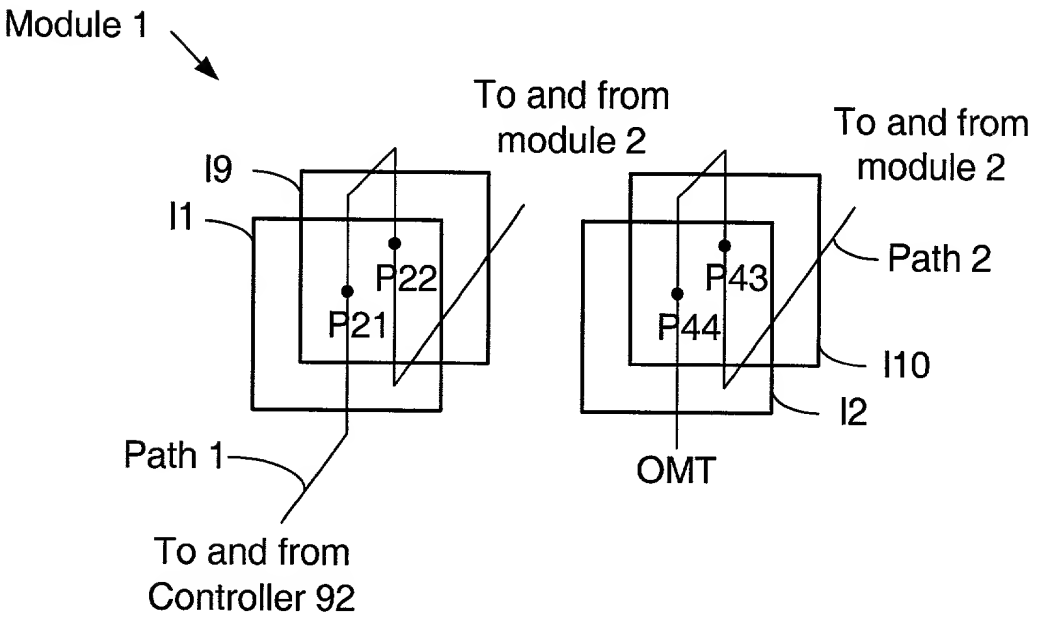
Module 1
To and from
module 2
To and from
module 2
I9
I1
P22
P21
P43
P44
Path 2
I10
I2
Path 1
OMT
To and from
Controller 92

FIG. 26

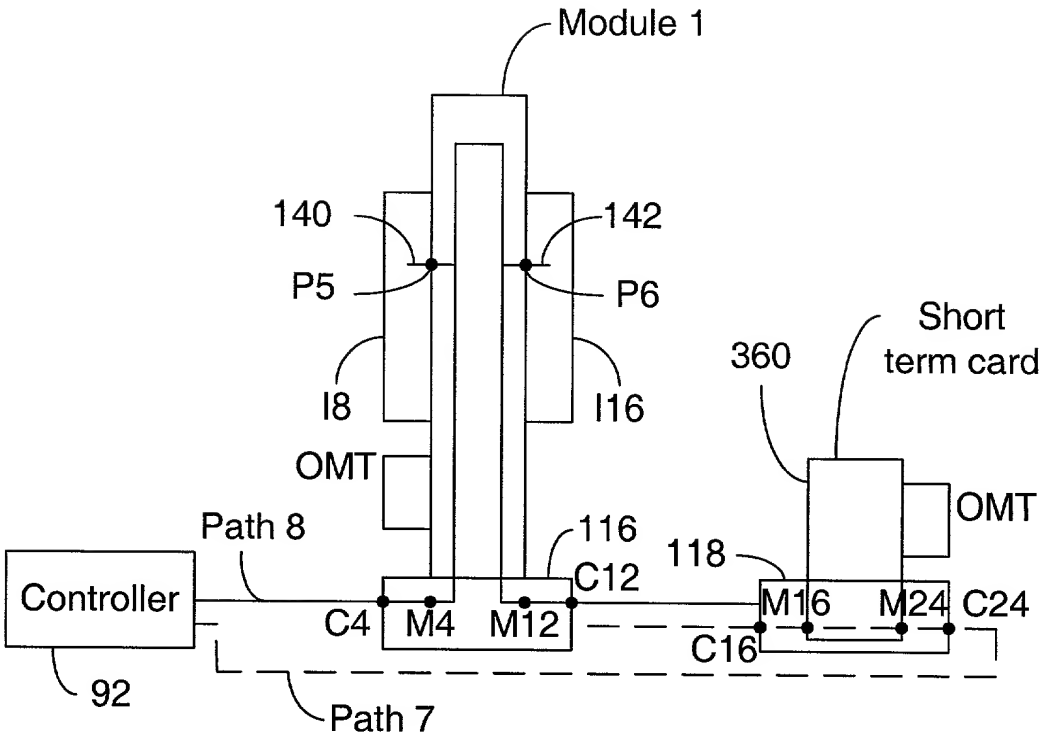
Module 1
140
142
P5
P6
I8
I16
OMT
Path 8
116
C12
Controller
C4
M4
M12
92
Path 7
360
Short
term card
OMT
118
M16
M24
C24
C16

FIG. 27

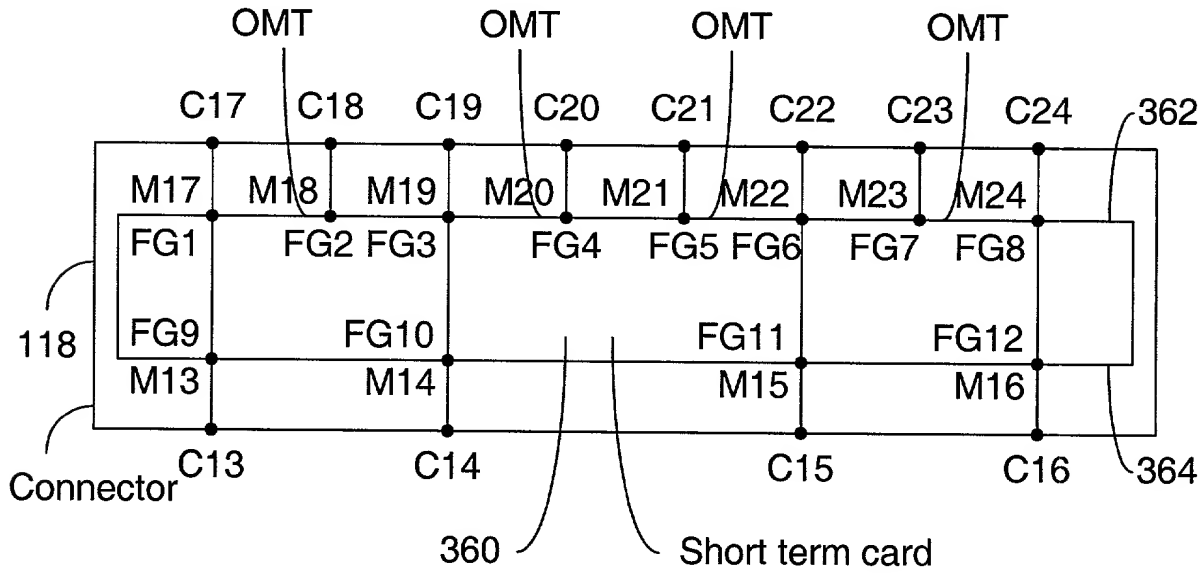
OMT
OMT
OMT
OMT
C17
C18
C19
C20
C21
C22
C23
C24
362
M17
M18
M19
M20
M21
M22
M23
M24
FG1
FG2
FG3
FG4
FG5
FG6
FG7
FG8
118
FG9
FG10
FG11
FG12
M13
M14
M15
M16
Connector
C13
C14
C15
C16
364
360
Short term card

FIG. 28

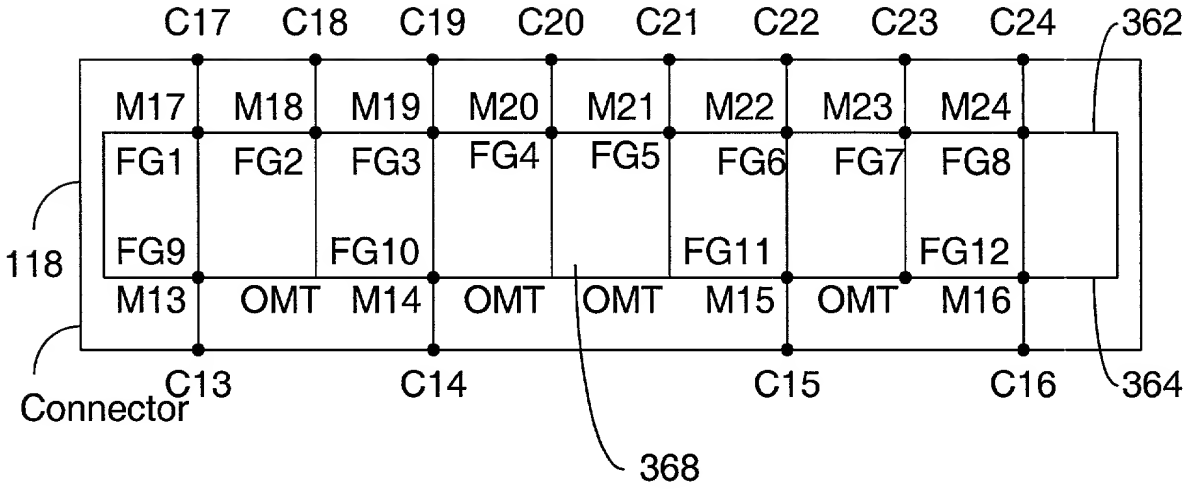
C17
C18
C19
C20
C21
C22
C23
C24
362
M17
M18
M19
M20
M21
M22
M23
M24
FG1
FG2
FG3
FG4
FG5
FG6
FG7
FG8
118
FG9
FG10
FG11
FG12
M13
OMT
M14
OMT
OMT
M15
OMT
M16
Connector
C13
C14
C15
C16
364
368

FIG. 29

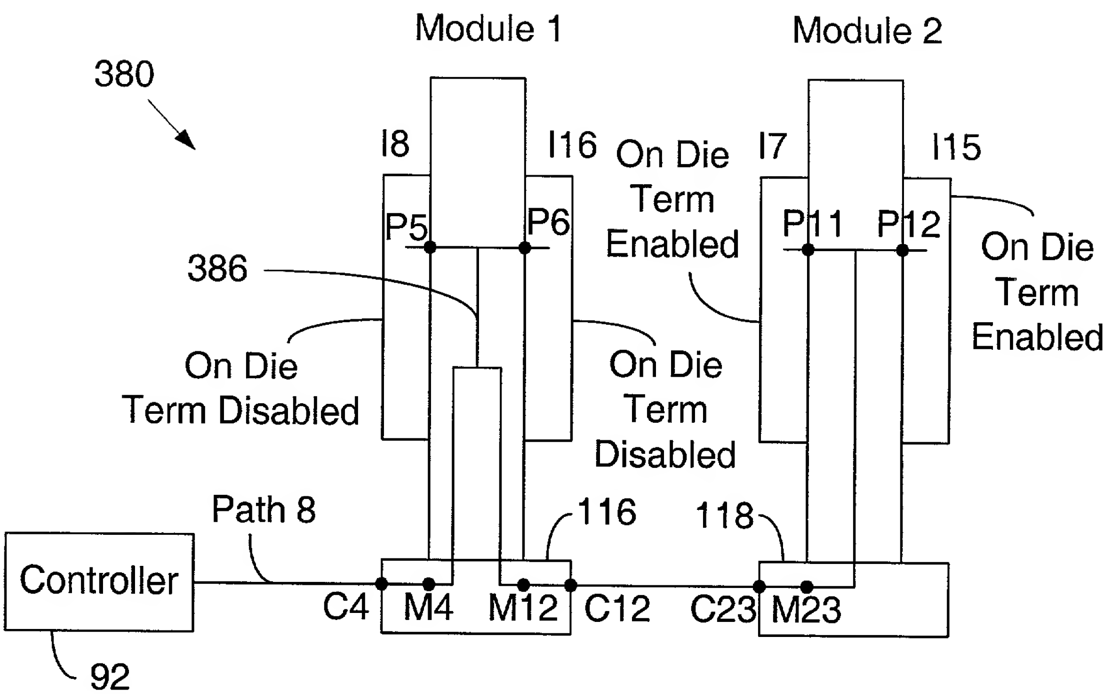
Module 1
Module 2
380
I8
I16
On Die Term Enabled
I7
I15
P5
P6
P11
P12
On Die Term Enabled
386
On Die Term Disabled
On Die Term Disabled
Path 8
116
118
Controller
C4
M4
M12
C12
C23
M23
92

FIG. 30

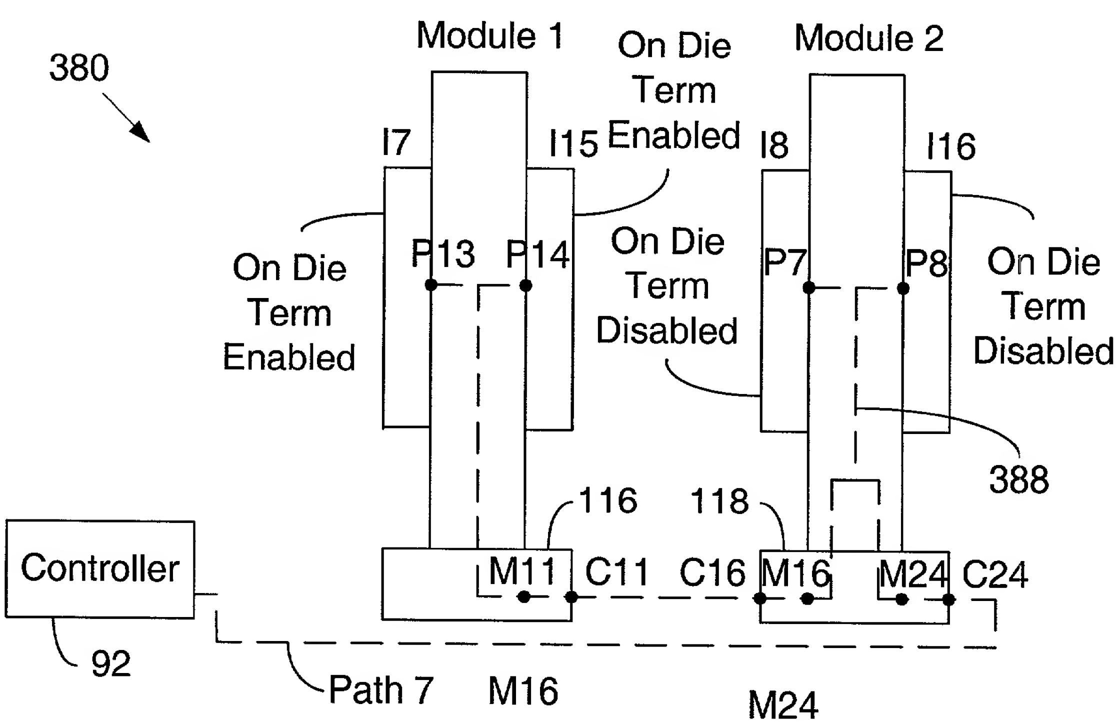
Module 1
On Die Term Enabled
Module 2
380
I7
I15
I8
I16
On Die Term Enabled
P13
P14
On Die Term Disabled
P7
P8
On Die Term Disabled
388
116
118
Controller
M11
C11
C16
M16
M24
C24
92
Path 7
M16
M24

FIG. 31

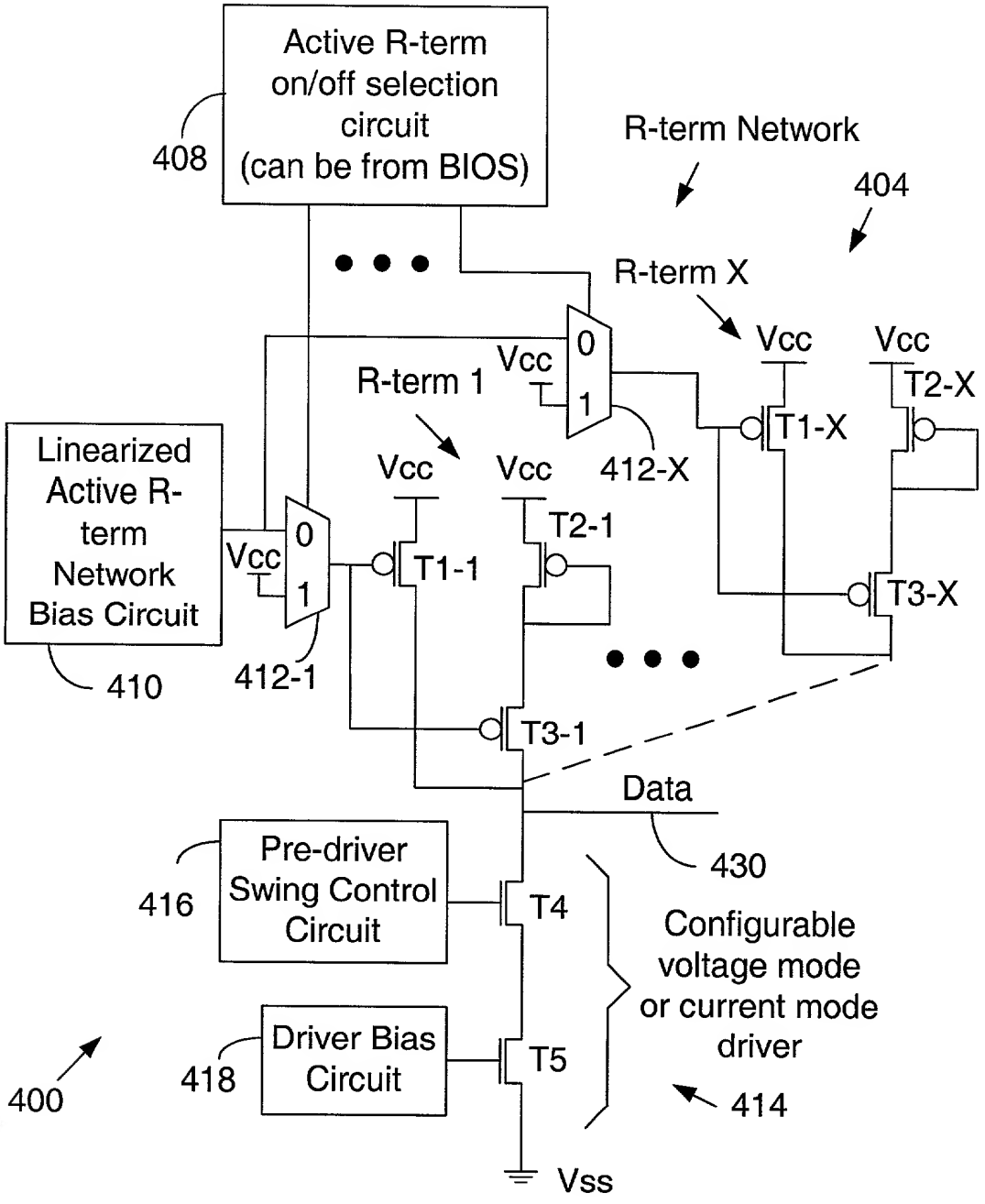
Active R-term on/off selection circuit (can be from BIOS)
408
R-term Network
404
R-term X
R-term 1
Vcc
0
1
412-X
T1-X
T2-X
Linearized Active R-term Network Bias Circuit
410
412-1
T1-1
T2-1
T3-X
T3-1
Data
430
Pre-driver Swing Control Circuit
416
T4
Configurable voltage mode or current mode driver
414
Driver Bias Circuit
418
T5
400
Vss

FIG. 32

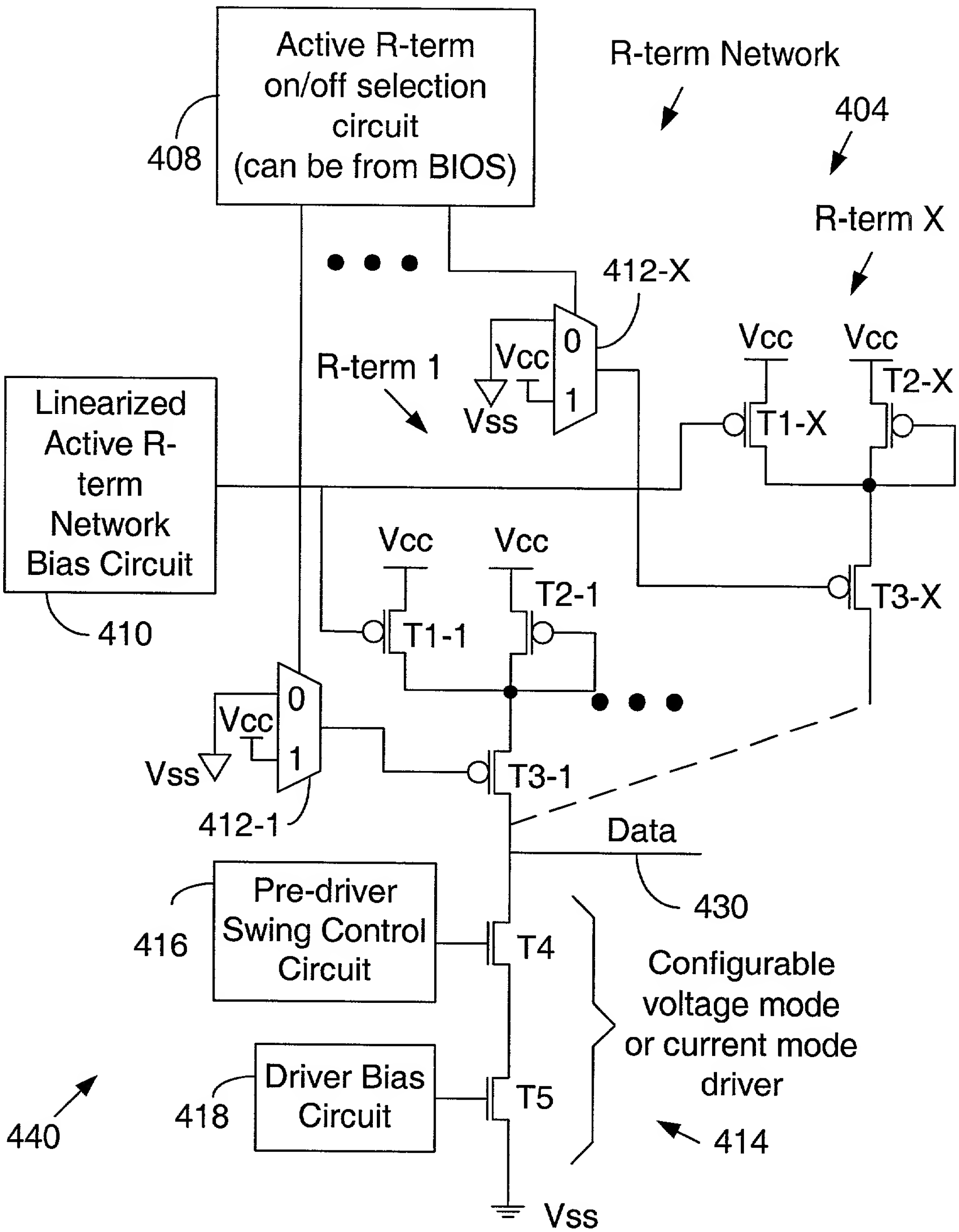
Active R-term on/off selection circuit (can be from BIOS)
408
R-term Network
404
R-term X
412-X
0
1
Vcc
Vss
R-term 1
Vcc
Vcc
T1-X
T2-X
Linearized Active R-term Network Bias Circuit
410
Vcc
Vcc
T2-1
T1-1
T3-X
0
1
Vcc
Vss
412-1
T3-1
Data
430
Pre-driver Swing Control Circuit
416
T4
Configurable voltage mode or current mode driver
Driver Bias Circuit
418
T5
440
414
Vss

FIG. 33

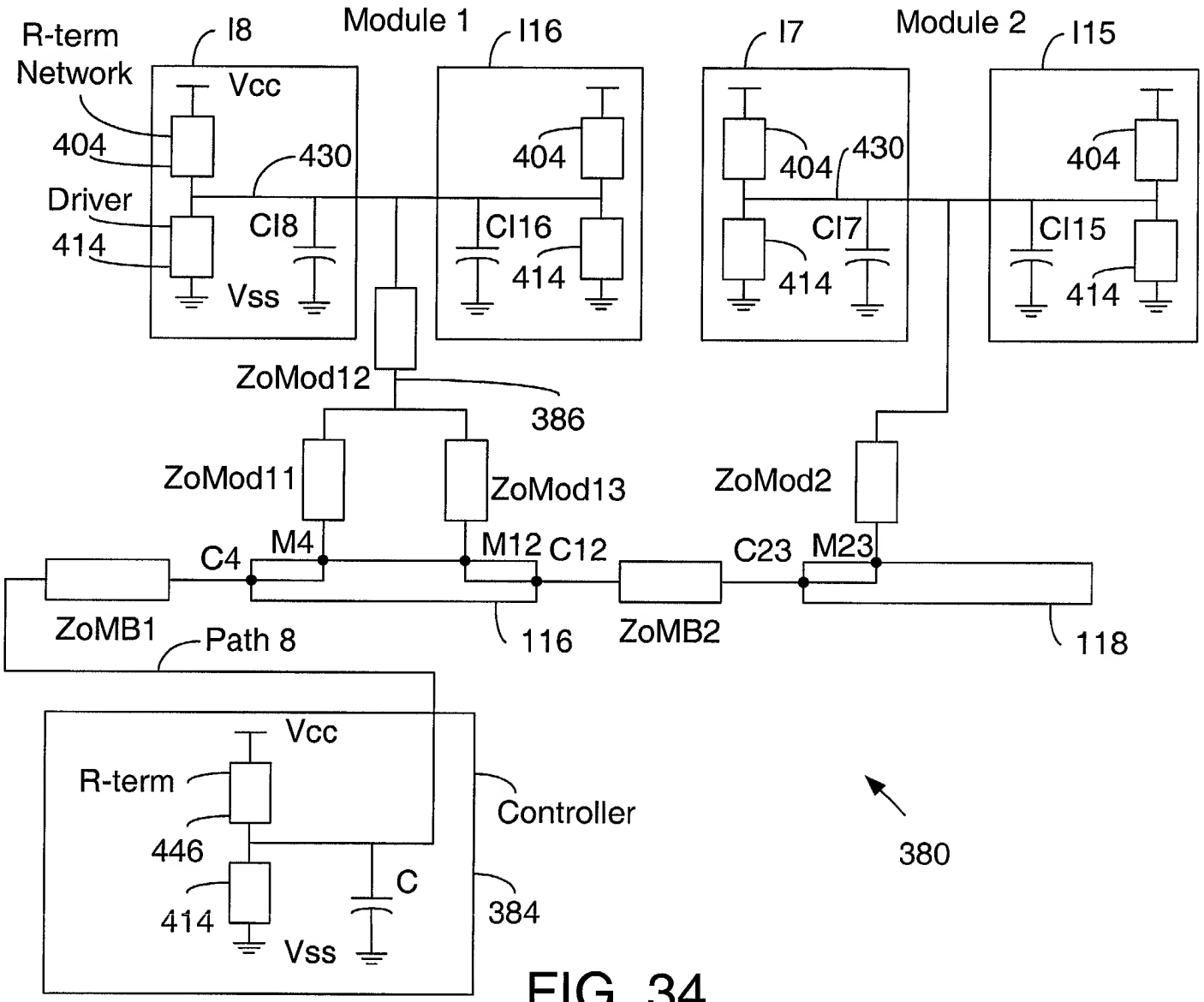

FIG. 34

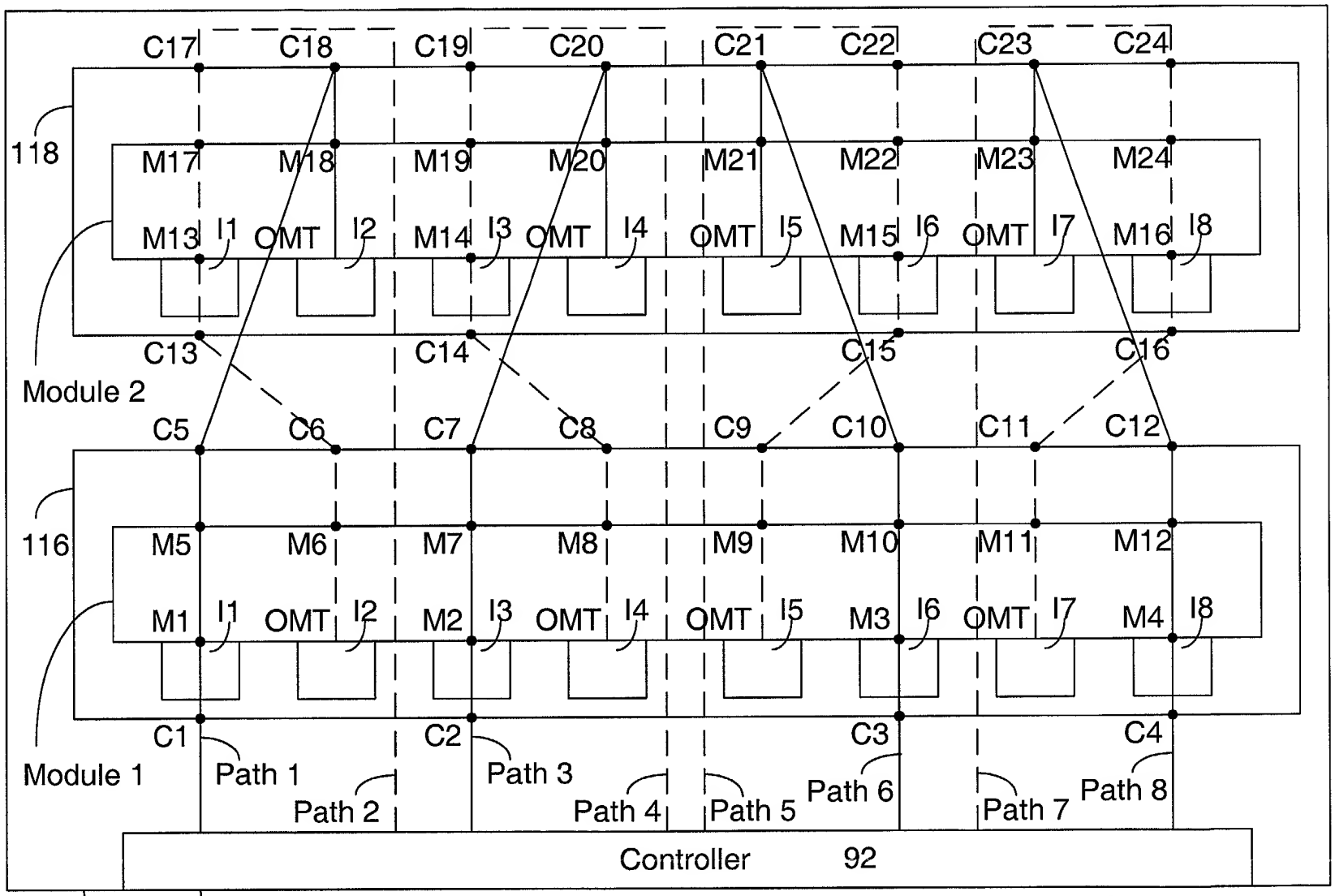

FIG. 35

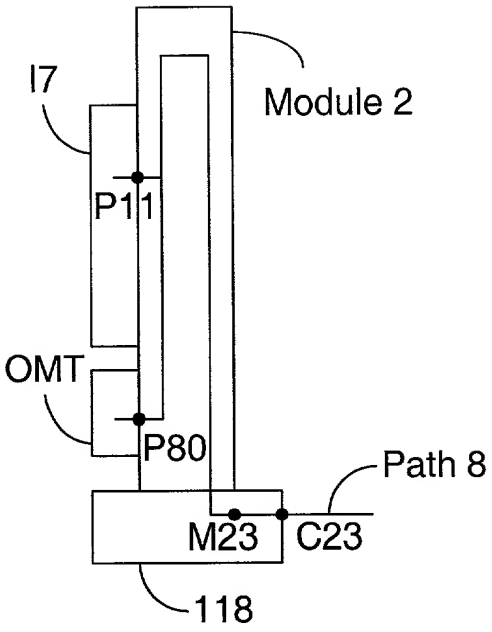

FIG. 36

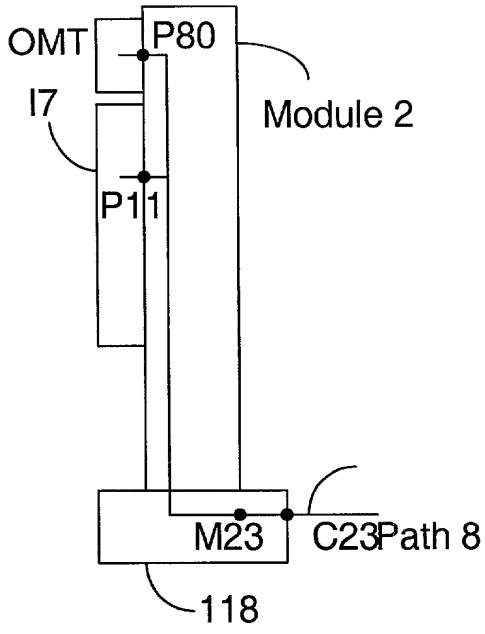

FIG. 37

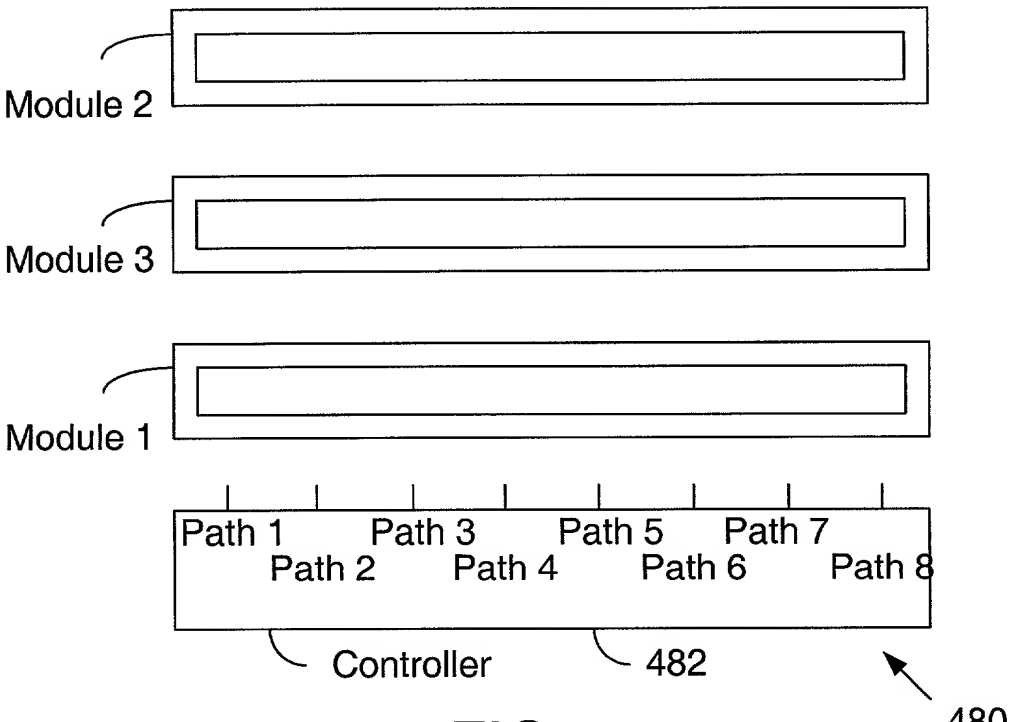

FIG. 38

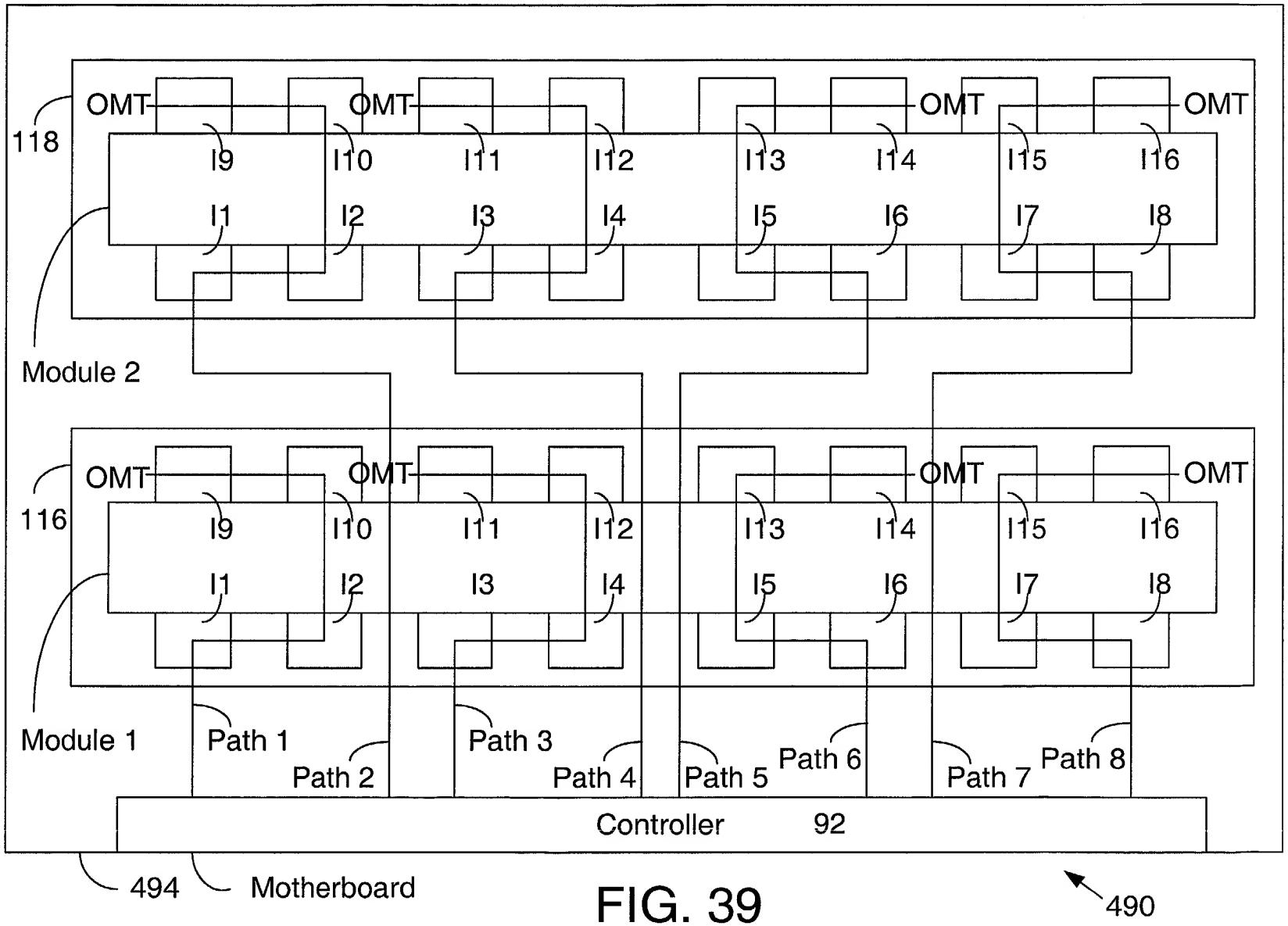

FIG. 39